Answer the questions in learning suite regarding the behavior of this memory.

// Declare multi-dimensional logic array (8 words, 8 bits each)

logic [7:0] register[7:0];

// Initialize the eight words

integer i;

initial

for (i=0;i<8;i=i+1)

register[i] = 0;

always\_ff@(posedge clk) begin

read1 <= register[addr1];

read2 <= register[addr2];

if (write) begin

register[writeAddr] <= writeData;

if (addr1 == writeAddr)

read1 <= writeData;

if (addr2 == writeAddr)

read2 <= writeData;

end

end

Demonstrate your understanding of the operation of the multi-port memory by completing the waveform above in the learning suite exam.

module **regfile**(clk, readReg1, readReg2, writeReg, writeData, write, readData1, readData2);

input wire logic clk;

input wire logic [4:0] readReg1, readReg2, writeReg;

input wire logic [31:0] writeData;

output logic write;

output logic [31:0] readData1, readData2;

How many total bits are there in this register file?

* 1024